DATA SHEET

M8192A Multi-Channel Synchronization Module

for M8190A and M8121A AWGs and M8030A Multi-Channel BERT

Features and benefits

- Synchronization of up to six M8190A or M8121A modules (= 12 channels)[1]
- One trigger input can trigger up to six M8190A or M8121A modules with deterministic latency
- Skew calibration with 50 fs delay resolution between any two channels
- 1U AXIe module for high port density

Description

The Keysight Technologies, Inc. M8192A synchronization module is used in conjunction with two to six M8190A or M8121A Arbitrary Waveform Generator modules to build a fully synchronous, phase coherent multi-channel generator system with up to 12 analog channels and 24 marker outputs.

When running in synchronous mode, all of the M8190A or M8121A modules work with the same sample clock and start at the same time. One of the AWGmodules is designated as the “master” module. The common sample clock is derived either from the master module’s internal clock synthesizer or from an external sample clock that is connected to the master module’s sample clock input.

Using the fine delay adjust capability of the M8190A or M8121A with 50 fs resolution, the skew can be adjusted to less than 1 ps between any two channels. Once adjusted, the skew is maintained across loading new waveforms, changing sample rate and power cycles.

A common trigger input is available on the synchronization module to trigger all the connected AWG modules simultaneously with deterministic latency. Triggered waveforms have the same inter-channel skew as continuous wave- forms. To achieve the lowest possible trigger delay uncertainty, the trigger input can be synchronized externally to the SYNC CLK output.

[1] M8190A and M8121A modules cannot be mixed; all modules connected to the M8191A must be of the same model number.

Applications

Typical applications include:

- Phase coherent multi-channel I/Q signal generation with up to six I/Q pairs
- Phase coherent multi-channel IF/RF generation with up to 12 IF/RF signals
- Multi-lane serial applications
- Physics research

Configurations

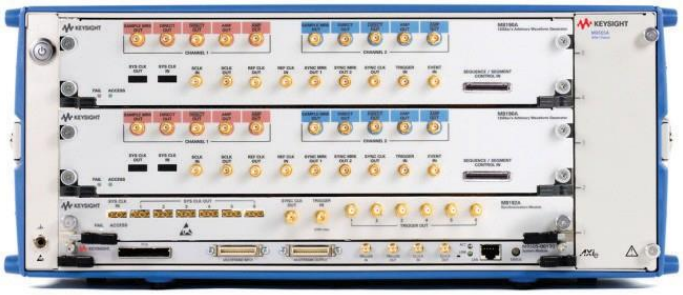
The M8192A can be used to synchronize M8190A or M8121A modules that are located within the same or different AXIe chassis. This allows very flexible configurations to address a variety of application requirements.

Trigger and clock connections are routed through special cables that are connected on the front panel between the M8192A module and the M8190A or M8121A modules.

For all system configurations except the 13-slot chassis setup, an external PC or laptop with PCIe cable connection is required to control the setup. In case of multiple AXIe chassis configurations, a desktop PC with two or three PCIe adapters is required. With a 13-slot AXIe chassis, an embedded controller can be used with up to five M8190A or M8121A modules.

The following configurations are possible:

- Up to 4 analog channels: One M9505A 5-slot AXIe chassis, one M8192A and two M8190A or M8121A modules.
- This configuration can also be ordered as a pre-configured M8190S Multichannel Arbitrary Waveform Generator System (applies to M8190A modules only)



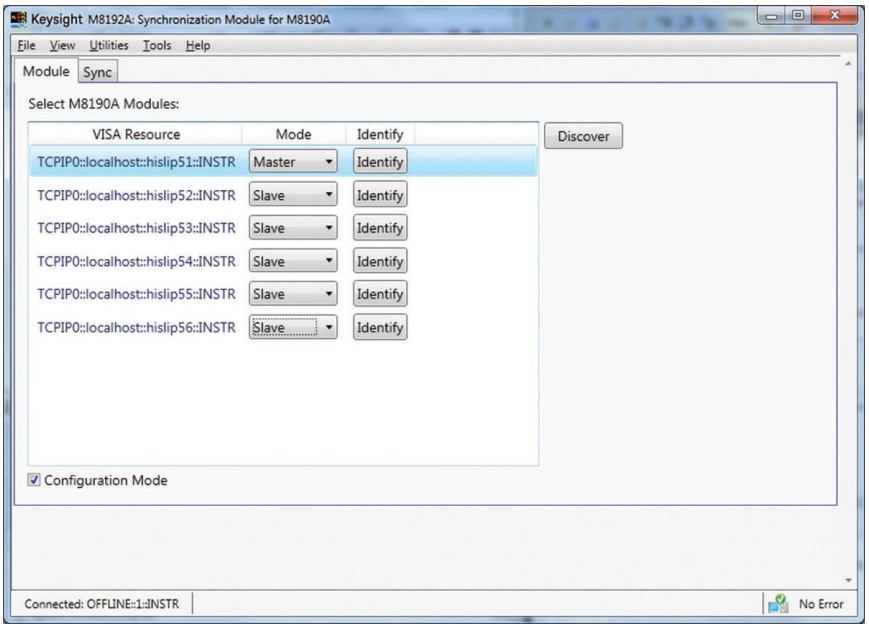
- Up to 8 analog channels: Two M9505A 5-slot AXIe chassis, one M8192A and three or four M8190A or M8121A modules.
- This configuration can also be ordered as a pre-configured M8190S Multichannel Arbitrary Waveform Generator System (applies to M8190A modules only).

- Up to 12 analog channels: Three M9505A 5-slot AXIe chassis, one M8192A and five or six M8190A or M8121A modules.

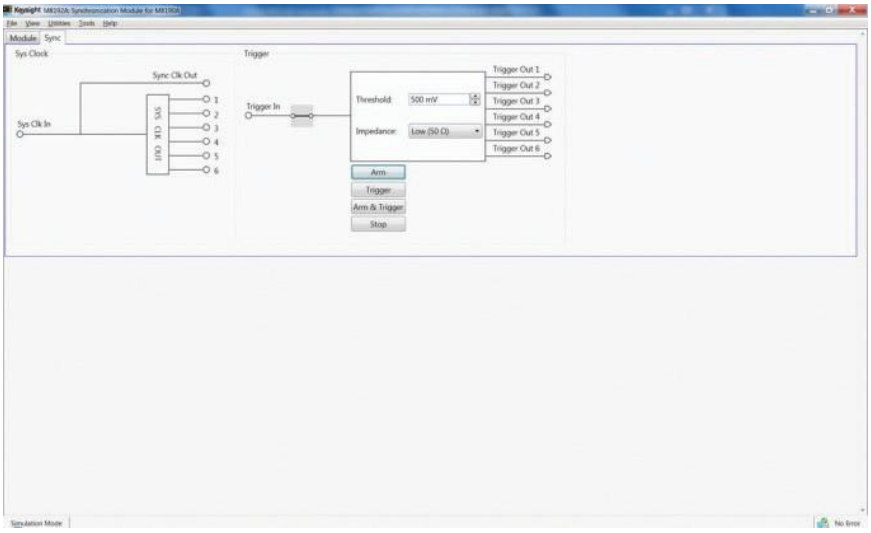
Software

The M8192A module has its own firmware and SFP (Soft Front Panel) - similar to the AWG modules - that allows you to control the trigger mode, trigger level and common start/stop of the multi-module setup. The SFP can be used to configure the entire synchronous system.

The firmware also offers a remote programming interface based on an IVI driver or SCPI commands.



Configuration screen of M8192A SFP



Clock and trigger distribution screen

Ordering Information

Product #	Description
M8192A	Synchronization Module for up to six M8190A AWG modules. Please note that two clock cables and two trigger cables are included. For more than two modules, the corresponding number of clock cables and trigger cables needs to be ordered separately.
M8192A-801	Clock Cable for the Synchronization Module (M8192A) (required for configurations with three or more M8190A modules)
M8192A-802	Trigger Cable for the Synchronization Module (M8192A) (required for configurations with three or more M8190A modules)
System bundles	
M8190S	Multichannel Arbitrary Waveform Generator System - two multi-channel selections are available
4-channel system	Consists of one M9505A 5-slot AXIe chassis (M8190S-B04), one M8192A synchronization module and two M8190A AWG modules, including the required number of clock and trigger cables (PCIe connectivity accessories will be added automatically)
8-channel system	Consists of two M9505A 5-slot AXIe chassis (M8190S-B08), one M8192A synchronization module and four M8190A AWG modules, including the required number of clock and trigger cables (PCIe connectivity accessories will be added automatically)
M8030A	Multi-Channel BERT System with up to 10 x 16 Gb/s
M8051A-802	Clock crossover distribution cable for M8051A (re-order product number for M8041-61614)

For M8190A or M8121A options and ordering information, please see the M8190A or M8121A data sheets, respectively.

Specifications for M8190A or M8121A

Sys Clock Input (from master AWG module)		
Connector and cable type	Proprietary multi-coax (M8192A-801)	
Clock rate	1 GHz to 12 GHz (configured in master AWG module)	
Sys Clock Output (to slave AWG modules)		
Connector and cable type	Proprietary multi-coax (M8192A-801)	
Sync Clock Output		
	M8190A	M8121A
Frequency		
• 14 Bit mode	Sample clock output frequency of M8190A divided by 48	Sample clock output frequency of M8121A divided by 64
• 12 Bit mode	Sample clock output frequency of M8190A divided by 64	Sample clock output frequency of M8121A divided by 64
• Interpolation mode	Sample clock output frequency of M8190A divided by (24 * interpolation factor)	Sample clock output frequency of M8121A divided by 32
Output amplitude	1.0 Vpp (nom) into 50 Ω	
Impedance	50 Ω (nom), AC coupled	
Connector type	SMA	
Trigger Input		
Input range	–5 V to +5 V	
Threshold		
• Range	–5 V to +5 V	
• Resolution	100 mV	
• Sensitivity	200 mV	
Polarity	Positive	
Input impedance	Selectable 1 kΩ or 50 Ω (nom)	
Max toggle frequency	Sync clock output frequency divided by 5	
Minimum pulse width		
• Asynchronous timing between Trigger Input and Sync Clock Output	1.1 * sync clock output period	
• Synchronous timing between Trigger Input and Sync Clock Output	1.0 * sync clock output period	
Connector type	SMA	
Trigger Output (to slave AWG modules)		
Connector and cable type	Proprietary coax (M8192A-802)	

Initial skew	Between any two channels in a multi-channel setup	
	M8190A	M8121A
Accuracy	± 20 ps (without system level calibration)	± 50 ps (nom) (without system level calibration)
Repeatability	2 ps (after changes of sample rate or power cycle)	2 ps (nom) without channel synchronization in between repeats[2,3] 20 ps (nom) with channel synchronization in between repeats[2,3]
Delay resolution for skew calibration	50 fs (see M8190A or M8121A data sheet)	

Specifications for M8030A

Sys Clock Input (from master M8041A module)	
Connector and cable type	Proprietary multi-coax (M8041-61614)
Sys Clock Output (to slave M8051A modules)	
Connector and cable type	Proprietary multi-coax (M8192A-801)
Initial skew	**Between any two channels in a multi-channel setup**
Accuracy	± 20 ps (without system level calibration)
Repeatability	2 ps (after changes of sample rate or power cycle)
Delay resolution for skew calibration	50 fs (see M8190A data sheet)

[2] Variable delay is set to 0 ps, the channels are in coupled mode, and the same amplifier path for both channels is selected. Skew is measured on a real-time oscilloscope with averaging enabled.

[3] Channel synchronization is performed upon sample frequency or sample mode (i.e. 14- or 12-bit) change, and can introduce channel-to-channel skew variability.

Timing Characteristics

The M8192A can operate synchronously or asynchronously. Synchronous operation must be selected to achieve minimum delay uncertainty between Trigger Input and Direct Out or Marker Out. For synchronous operation Trigger Input must be synchronous to the Sync Clock Output[4].

Characteristics	Description	
	M8190A	M8121A
Setup time (Trigger Input to rising edge of Sync Clock Output)	+ 3.4 ns (typ)	+ 3.4 ns (typ)
Hold time (Rising edge of Sync Clock Output to Trigger Input)	–1.1 ns (typ)	–1.1 ns (typ)
Delay in 12 bit mode (Trigger Input (M8192A) to Direct Out of AWG)	10240 external sample clock cycles + 0.5 internal sample clock cycles[5] + 8.5 ns (meas)	4022.4 * sample clock period + 29.0 ns + 8.5 ns (meas)
Delay in 14 bit mode (Trigger Input (M8192A) to Direct Out of AWG)	7680 external sample clock cycles + 0.5 internal sample clock cycles + 8.5 ns (meas)	4022.4 * sample clock period + 29.0 ns + 8.5 ns (meas)
Delay in interpolation mode (Trigger Input (M8192A) to Direct Out of AWG)	Interpolation factor * 3840 external sample clock cycles + 4.5 internal sample clock cycles[1] + 8.5 ns (meas)	TBD[6]
Delay uncertainty (asynchronous mode)	1 sync clock output cycle[7]	
Delay uncertainty (synchronous mode)	10 ps (typ)	< sample clock period (nom)

[4] Refer to Sync clock output specifications for the ratio between Sample clock output frequency and Sync clock output frequency.

[5] For the definition of the internal sample clock, refer to the data sheet of the M8190A section ‘Sample clock input’.

[6] Requires option DUC. Please contact Keysight for availability on the M8121A.

[7] Refer to Sync clock output specifications for the ratio between Sample clock output frequency and Sync clock output frequency.

General

Characteristics	Description
Power consumption	60 W
Operating temperature	0 °C to +40 °C
Operating altitude	Up to 2000 m
Operating humidity	5% to 80% relative humidity, non-condensing
Storage temperature	–40 °C to +70 °C
Interface to controlling PC	PCIe (see AXIe chassis specification)
Form factor	1-slot AXIe module
Dimensions (W x H x D)	351 x 29 x 310 mm
Weight	3.1 kg
Safety designed to	IEC61010-1, UL61010, CSA22.2 61010.1 tested
Warm-up time	30 min
Calibration interval	2 years recommended
Cooling requirements	When operating the M8192A, choose a location that provides at least 80 mm of clearance at rear, and at least 30 mm or clearance at each side

Definitions

Characteristics	Description
Specification (spec)	The warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 °C to 40 °C and after a 45-minute warm up period. Within ± 10 °C after autocal. All specifications include measurement uncertainty and were created in compliance with ISO-17025 methods. Data published in this document are specifications (spec) only where specifically indicated.
Typical (typ)	The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 23 °C).
Nominal (nom)	The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed. This data is not warranted and is measured at room temperature (approximately 23 °C).
Measured (meas)	An attribute measured during development for purposes of communicating the expected performance. This data is not warranted and is measured at room temperature (approximately 23 °C).
Accuracy	Represents the traceable accuracy of a specified parameter. Includes measurement error and timebase error, and calibration source uncertainty

Software

Characteristics	Description
Operating systems	Windows 7, 8.1, 10, 64-bit
Soft front panel	A graphical user interface (GUI or soft front panel) is offered to control all functionality to the instrument. It contains screens for controlling clock, outputs, marker, trigger, sequencer, importing waveforms and creating standard waveforms.
SCPI language	Remote control via SCPI
IVI-driver	An IVI-COM driver as well as IVI-C driver will be provided
LabView-driver	A LabView driver will be provided

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